Minicomputer

WEISMANTEL

WAICOM–16*

SYSTEM CONFIGURATOR

*Trademark of Weismantel Associates, Inc.

WEISMANTEL WAICOM-16

The WAICOM-16 processor is a 16-bit medium-scale digital processor constructed using integrated circuit logic and featuring a memory cycle and basic instruction execution time of 500 nsec. It has an instruction repertoire of 83 instructions. The processor contains a multi-task feature which allows any one of a number of task programs to be called up and executed under hardware control as directed by an executive routine. The memory is expandable from 8K words to 65K words in increments of 8K words. A feature to allow two processors or several devices to access memory is provided by the multiple access controller (MAC) unit which adds additional memory access paths to each 8K module up to a total of four paths to each module. The standard WAICOM instruction set includes hardware multiply and divide. Additional arithmetic capabilities are provided by an optional Expanded Arithmetic Unit (EAU), which provides double-precision fixed-point and single and double-precision floating-point instructions.

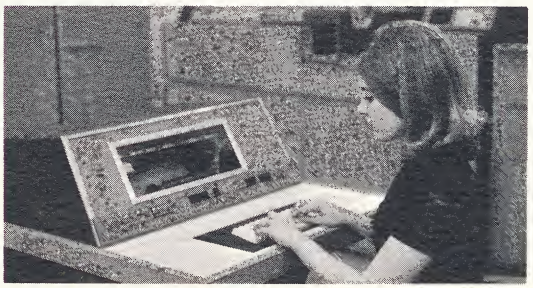
The processor permits interfacing with a wide variety of peripheral devices for which the I/O section provides particular addressing modes depending on the peripheral device used. The Processor Specified Control mode is used for peripherals which do not multiplex several devices into one channel. The Subsystem Specified Control mode is used for multiplexing several peripheral devices onto one I/O channel. Subsystem Specified Address mode enables the peripheral device to specify directly the memory address at which data will be either read or stored. This mode permits external data to be combined in particular combinations with data already stored at the address location, as follows; external data ANDed with memory data, external data ORed with memory data, or external data ADDed to memory data. The number of I/O channels on the processor is modular, with four channels in the basic processor. Expansions in increments of one channel to a maximum of 16 channels are available as options. An option is available to provide paging of I/O data transfers. The installation of the multi-task option is a prerequisite to installation of the I/O paging option. An additional option is available to provide hardware registers for holding control words used in control of I/O transfers.

Two particularly significant features of the system are modular multi-processor addressing and hardware-controlled multi-task paging. Multi-processor addressing is provided by the multiple access controller (MAC), which allows two processors to access memory by providing additional access paths on a modular basis. A MAC is located in each 32K memory cabinet, and provides up to four access paths to each of the four 8K memory modules in the memory cabinet. This capability is provided by a basic MAC configuration, which contains two access paths and one memory path to one 8K module. These paths are field expandable to four access paths and four memory paths, the maximum MAC configuration.

Paging of the multi-task option provides linking of multiple tasks fragmented throughout memory under complete hardware control. Once initiated by the executive program, linking of the task segments is performed under hardware control by the processor logic. This feature relieves the programmer of the responsibility of keeping track of the location of various program segments.

The basic instruction repertoire includes load, store, memory modification, sequence modification, logical operators, and input/output commands. The basic arithmetic instructions include single and double word add and subtract, single word multiply and divide, and binary coded decimal to binary conversion and vice versa. Double-precision multiply and divide, and floating point arithmetic are available as an option.

The basic processor has a single set of index and accumulator registers. The handling of multiple sets of index and accumulator registers for independent tasks is a software function. Multi-task operation, privileged instruction protection, code protection, memory protection, automatic index and accumulator store and restoration, and paging are available as a single option.



WAICOM-16 PROCESSOR

ARITHMETIC AND CONTROL SECTION

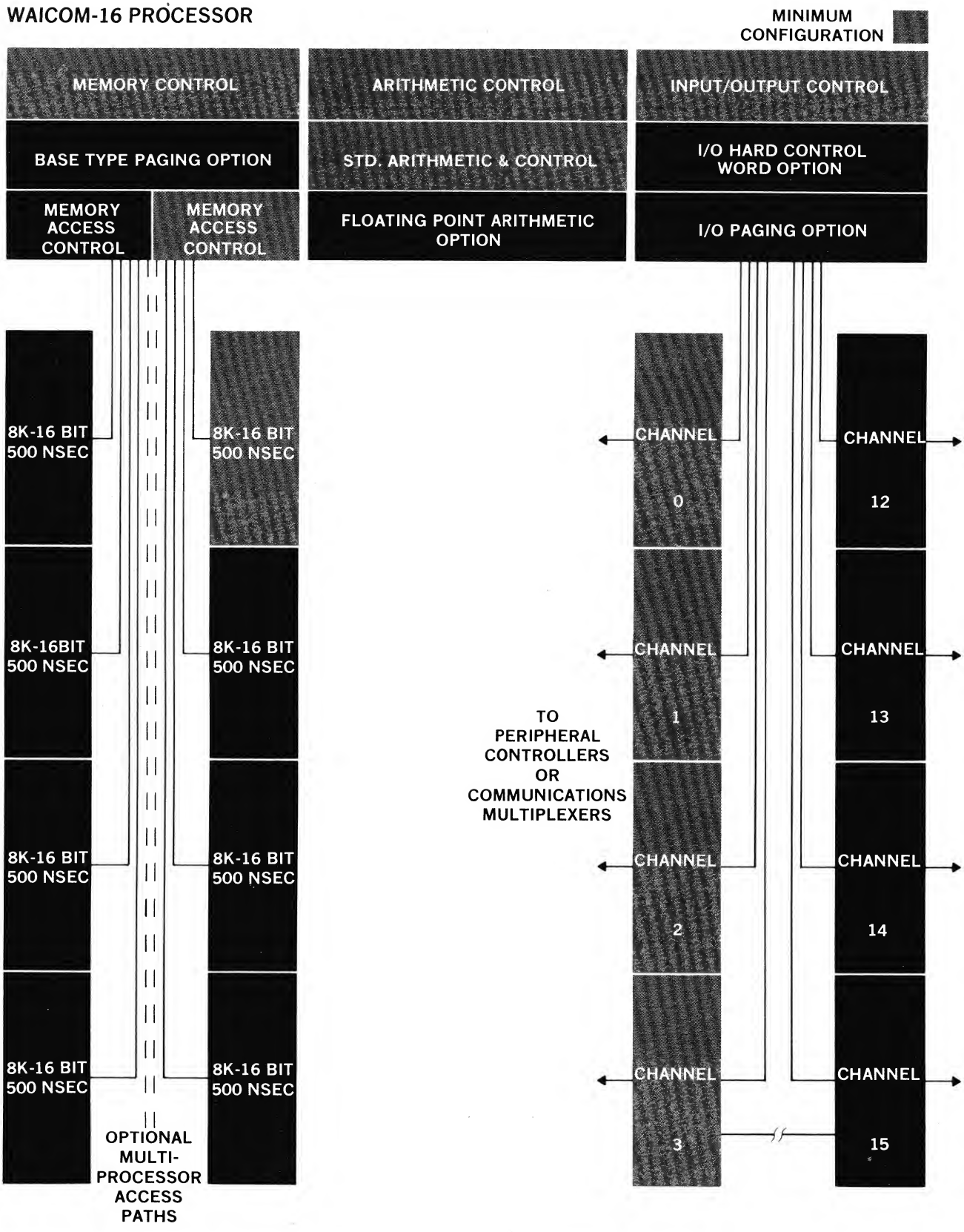
500 nanosecond basic Execution time
Overlapped instruction fetch And execution
10 Accumulators
6 Index Registers
Indirect Addressing
Real-time Clock
83 Standard Operations
Including: Multiply/Divide
Decimal-Binary Conversions
OPTIONAL: 32 And 64 bit floating point arithmetic.

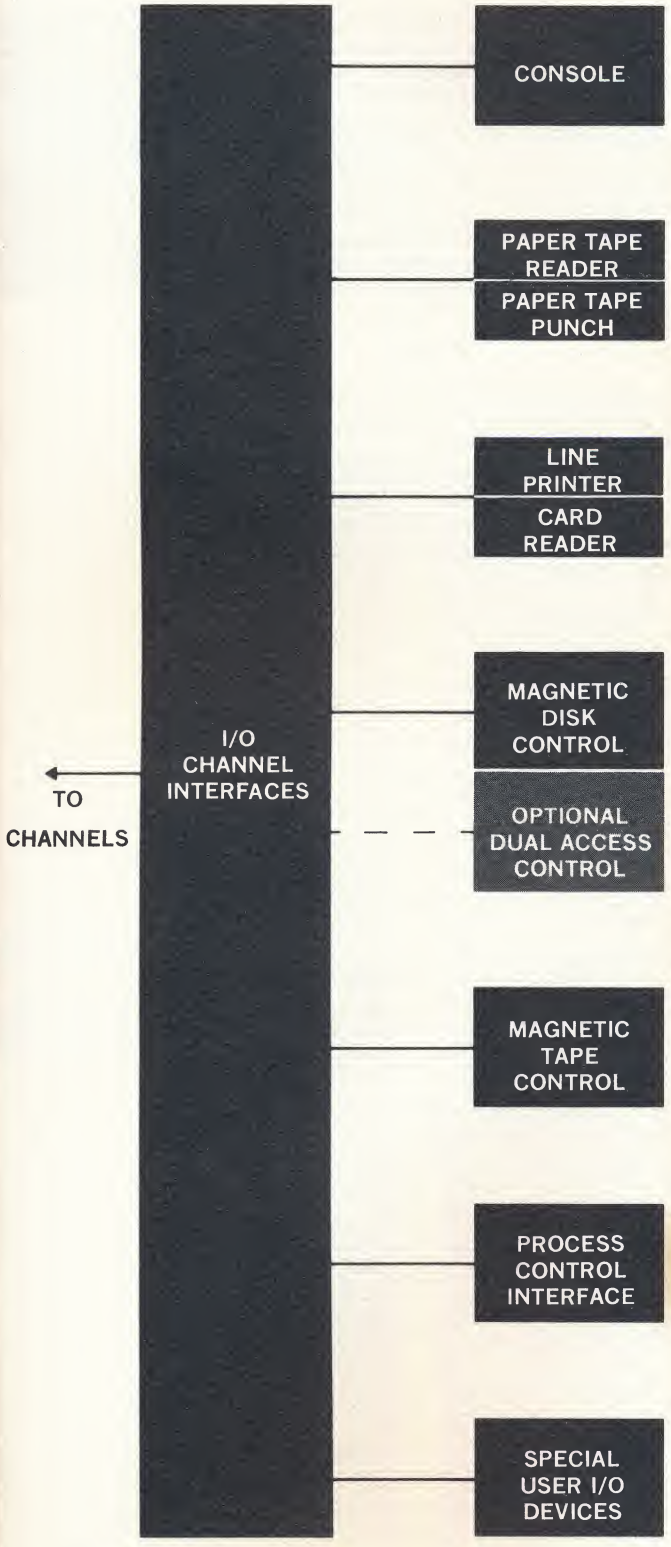
MEMORY CONTROL SECTION

500 nanosecond memory cycle time
16 bits data + 2 bits parity Per word
8K word minimum
Expandable To 65K In 8K modules
Separate access paths To each 8K module
OPTIONAL: multi-processer access path
base type paging

INPUT/OUTPUT CONTROL SECTION

4 I/O channels standard
Expandable To 16 channels
Overlap With other channels And instruction execution
2.0 million words/sec maximum transfer rate
Subsystem Specified Indexing
Automatic tabling Of communication interrupts
OPTIONAL: I/O paging option
I/O hard control word option


WAICOM-16 PROCESSOR
MINIMUM CONFIGURATION
MEMORY CONTROL
ARITHMETIC CONTROL
INPUT/OUTPUT CONTROL
BASE TYPE PAGING OPTION
STD. ARITHMETIC & CONTROL
I/O HARD CONTROL WORD OPTION
MEMORY ACCESS CONTROL
MEMORY ACCESS CONTROL
FLOATING POINT ARITHMETIC OPTION
I/O PAGING OPTION
8K-16 BIT 500 NSEC
8K-16 BIT 500 NSEC
8K-16BIT 500 NSEC
8K-16 BIT 500 NSEC
8K-16 BIT 500 NSEC
8K-16 BIT 500 NSEC
8K-16 BIT 500 NSEC
8K-16 BIT 500 NSEC
OPTIONAL MULTI-PROCESSOR ACCESS PATHS
CHANNEL 0
CHANNEL 12
CHANNEL 1
CHANNEL 13
CHANNEL 2
CHANNEL 14
CHANNEL 3
CHANNEL 15
TO PERIPHERAL CONTROLLERS OR COMMUNICATIONS MULTIPLEXERS



WAICOM-16 PERIPHERALS

OPERATORS CONSOLE

System Controls and Indicators
30 CPS Printer
55-Key Input Keyboard
OPTIONAL: Day clock

PAPER TAPE SUBSYSTEM

300 CPS Reader
25 CPS Punch

MAGNETIC DISK SUBSYSTEM

4 Drives per Controller maximum
20 Recording Surfaces
203 Access Arm Positions
20.8 Million Characters/Pack
57.5 Milliseconds average access
15 Milliseconds track to track access
2.5 Million bits/second transfer rate
OPTIONAL: Dual Access Controller

PRINTER SPECIFICATIONS

300 lines per minute
132 print positions
64 character
8 channel vertical control
6 or 8 lines per inch

READER SPECIFICATIONS

300 CPM Reader
Std. 80 column tab card size
Photoelectric sensing mechanism
Column binary capability

MAGNETIC TAPE SUBSYSTEM

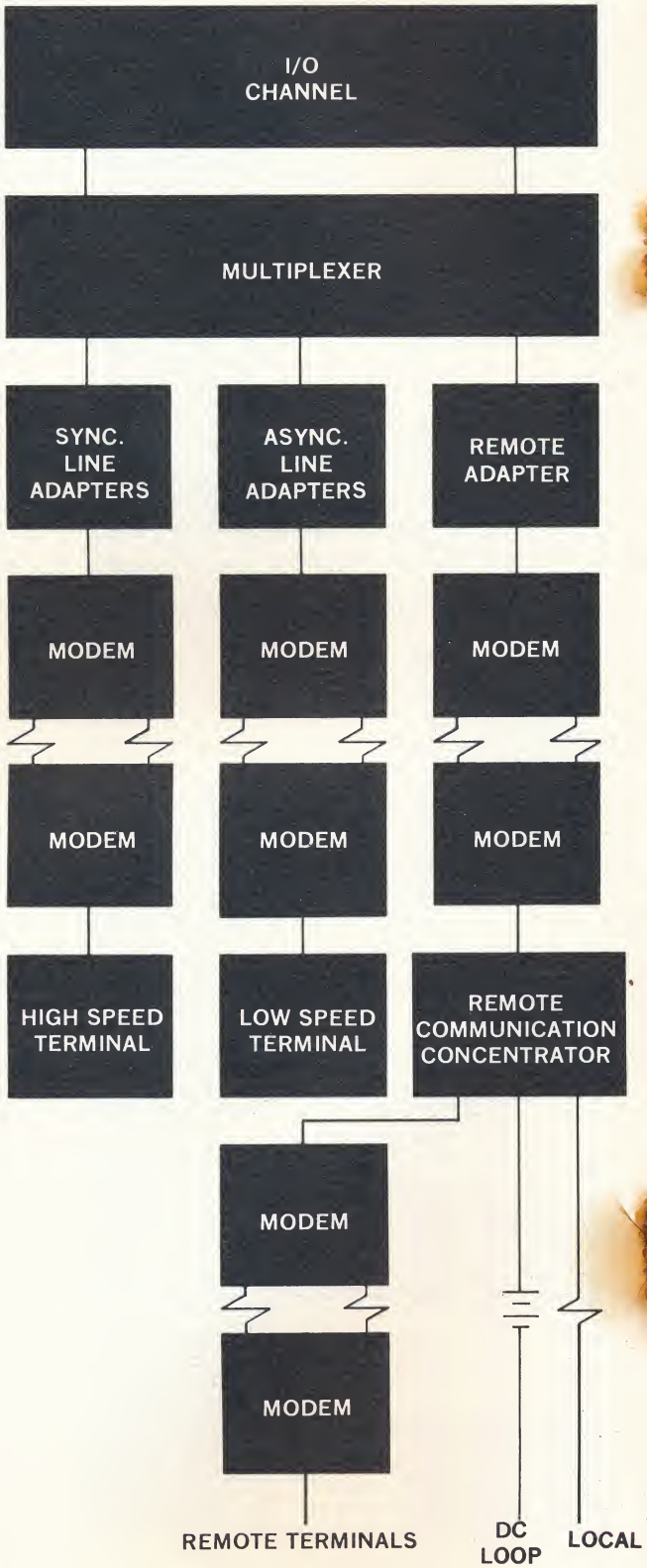
8 Transports per controller maximum
25 IPS Tape speed
800 BPI — 7 or 9 track — compatible
20 KC transfer rate
16 milliseconds average start time
25 milliseconds average stop time
OPTIONAL: 37.5 IPS tape speed
556 BPI recording density

PROCESS CONTROL I/O

A/D converters
D/A converters

SPECIAL USER I/O DEVICES

Plotters
Display devices
Other



WAICOM-16 COMMUNICATIONS I/O

Up to 256 lines total

MULTIPLEXERS

8 or 16 lines/multiplexer
Asynchronous or synchronous lines
385K char./sec aggregate burst rate
OPTIONAL: dialer/8 lines

MULTIPLEXER EXPANDER

4 multiplexers/expander maximum

LINE ADAPTERS (for above)

External interrupt generation
Character buffering and recognition
Late acknowledge detection
Ring indicator recognition
Loss of carrier recognition
Automatic dialing on a shared basis
Simplex, half duplex or full duplex modes

ASYNCHRONOUS LINE ADAPTER

Up to 3500 baud/sec.
5, 6, 7, 8-level codes
RS232 B/C and DC loop interfaces

SYNCHRONOUS LINE ADAPTER

Up to 230.4K baud/sec.
5, 6, 7, 8 level codes
RS232 B/C and current interfaces

REMOTE ADAPTER

Local site interface for RCC
Sorts & merges up to 32 lines in TDM
RS232 B/C interface
Requires 3 line positions

REMOTE COMMUNICATIONS CONCENTRATOR (RCC)

Time division multiplexer
Up to 32 low speed line input
110, 150, 165 baud/sec. asynchronous rates (intermixed)
RS232 B/C and DC loop interfaces
2000, 2400, 4800 baud/sec. synchronous output

WAICOM-16 OPERATING SYSTEM

The Disc Operating System consists of three basic groups — the Executive, the Language Processors, and the System Library.

EXECUTIVE
Provides orderly control and co-ordination of all tasks submitted for execution.

Job Control
Provides the scheduling, sequencing, and inter-program communication ability. By providing a relatively simple interface to the user, the Executive relieves the user of concern for the internal interaction between user program and other co-existant programs.

Facility Control
Provides a uniform mechanism for allocation of all system resources.

File Management
Provides extensive assistance to the user by maintaining a directory of files, protecting file integrity through controlled access, and providing a device — independent interface to file storage media.

I/O Control
Provides a method of orderly control of all I/O service requests. It provides a standard interface for device handlers, and a priority-sensitive selection of methods of completion notification. I/O operations are organized to take full advantage of WAICOM-16 hardware abilities such as automatic command and data chaining; and hard/soft interrupts.

LANGUAGE PROCESSORS

FORTRAN
A language processor capable of compiling relocatable object programs and re-entrant sub-programs according to the language defined in ANS X3.9 - 1966; with extensions such as bit manipulation.

WAICOM-16 Assembler
Provides a simple method of generating WAICOM-16 instructions and data in symbolic form. It also contains standard procedures for interface with the Executive.

SYSTEM LIBRARY
Contains all elements of the Operating System not required to be normally resident in main storage. The user may participate extensively in its definition.

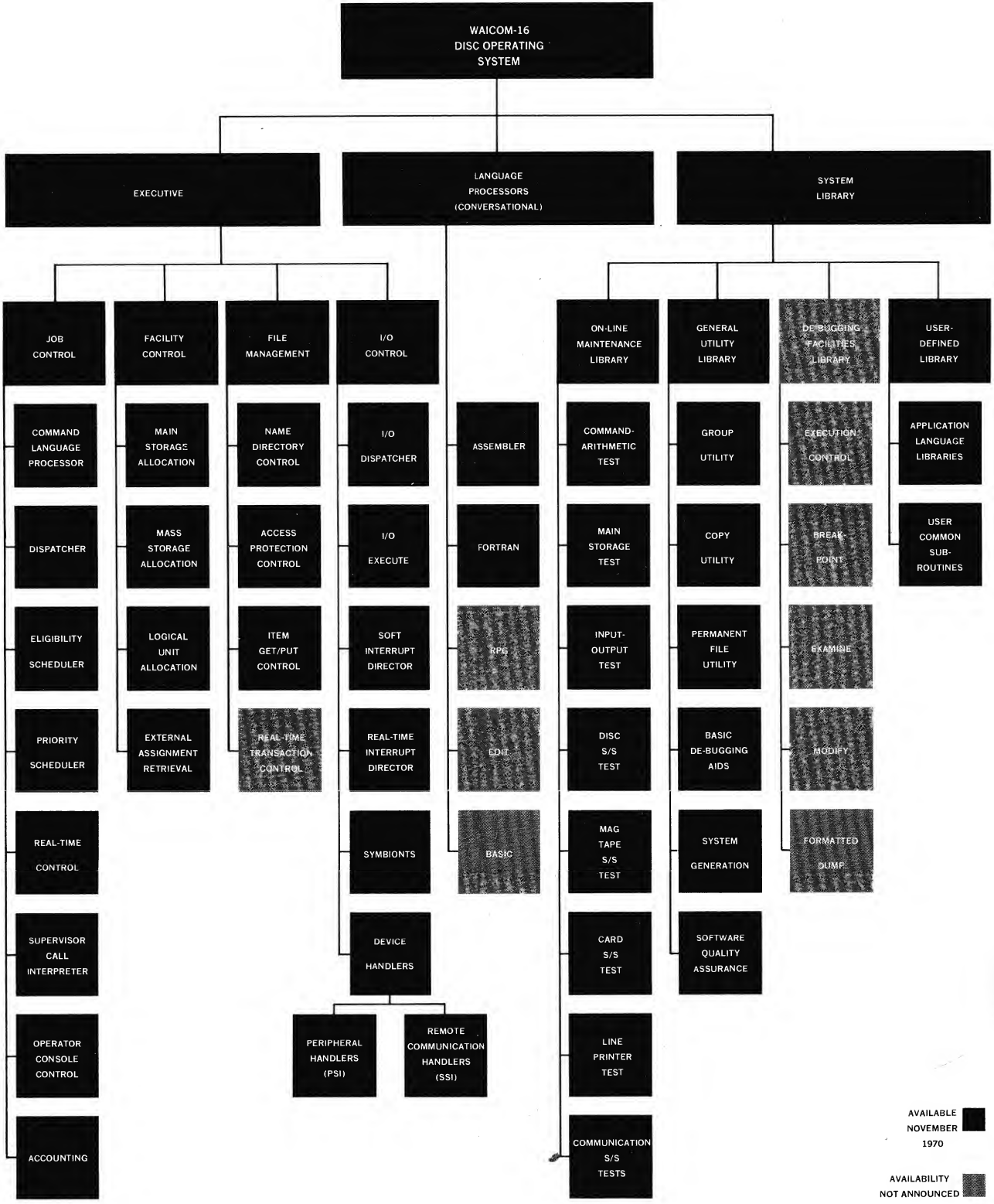
On-Line Maintenance Library
Provides all routines necessary to effect dynamic testing of any system hardware component under the control of the Operating-Systems.

General Utility Library
Provides routines for general file maintenance and modification, such as grouping, copying, etc. It also provides basic de-bugging aids: Dump, Modify, Search. In addition it supplies a collection of test packages designed to prove conformance to Operating System specifications.

User-Defined Library
Contains any collection of programs the user requires.

INSTRUCTION SET

MNEMONIC	EXEC. TIME (NSEC)[1]	DESCRIPTION
LX	500	Load X0
LX1	500	Load X1
LUX	500	Load Upper to X0
LLX	500	Load Lower to X0
SX	500	Store X0
SX1	500	Store X1
SUX	500	Store Upper from X0
SLX	500	Store Lower from X0
RAX	1200	Replace Add to X0
RMX	1200	Replace Masked X0
ROR	1200	Replace Selective Set
RNAND	1200	Replace Selective Clear
J	700[5]	Jump
LMJ	700[5]	Load Modifier and Jump
SEI	500/1000	Skip if Equal and Increment
JGD	500/700[5]	Jump if Greater and Decrement
LR	500/1000	Load R
SR	500/1000	Store R
LDR	900/1400	Load Double R
SDR	900/1400	Store Double R
OR	500/1000	OR R
AND	500/1000	AND R
XOR	500/1000	Exclusive OR R
NAND	500/1000	Negative OR R
TEP	500/1000	Test Even Parity
TOP	500/1000	Test Odd Parity
SLS	500[5]	Shift Left Single
SLD	900	Shift Left Double
SRS	500	Shift Right Single
SRD	900	Shift Right Double


WAICOM-16
DISC OPERATING
SYSTEM
EXECUTIVE
LANGUAGE
PROCESSORS
(CONVERSATIONAL)
SYSTEM
LIBRARY
JOB
CONTROL
FACILITY
CONTROL
FILE
MANAGEMENT
I/O
CONTROL
ON-LINE
MAINTENANCE
LIBRARY
GENERAL
UTILITY
LIBRARY
DE-BUGGING
FACILITIES
LIBRARY
USER-
DEFINED
LIBRARY
COMMAND
LANGUAGE
PROCESSOR
DISPATCHER
ELIGIBILITY
SCHEDULER
PRIORITY
SCHEDULER
REAL-TIME
CONTROL
SUPERVISOR
CALL
INTERPRETER
OPERATOR
CONSOLE
CONTROL
ACCOUNTING
MAIN
STORAGE
ALLOCATION
MASS
STORAGE
ALLOCATION
LOGICAL
UNIT
ALLOCATION
EXTERNAL
ASSIGNMENT
RETRIEVAL
NAME
DIRECTORY
CONTROL
ACCESS
PROTECTION
CONTROL
ITEM
GET/PUT
CONTROL
REAL-TIME
TRANSACTION
CONTROL
I/O
DISPATCHER
I/O
EXECUTE
SOFT
INTERRUPT
DIRECTOR
REAL-TIME
INTERRUPT
DIRECTOR
SYMBIONTS
DEVICE
HANDLERS
PERIPHERAL
HANDLERS
(PSI)
REMOTE
COMMUNICATION
HANDLERS
(SSI)
ASSEMBLER
FORTRAN
RPG
EDIT
BASIC
COMMAND-
ARITHMETIC
TEST
MAIN
STORAGE
TEST
INPUT-
OUTPUT
TEST
DISC
S/S
TEST
MAG
TAPE
S/S
TEST
CARD
S/S
TEST
LINE
PRINTER
TEST
COMMUNICATION
S/S
TESTS
GROUP
UTILITY
COPY
UTILITY
PERMANENT
FILE
UTILITY
BASIC
DE-BUGGING
AIDS
SYSTEM
GENERATION
SOFTWARE
QUALITY
ASSURANCE
EXECUTION
CONTROL
BREAK-
POINT
EXAMINE
MODIFY
FORMATTED
DUMP
APPLICATION
LANGUAGE
LIBRARIES
USER
COMMON
SUB-
ROUTINES
AVAILABLE
NOVEMBER
1970
AVAILABILITY
NOT ANNOUNCED

SRSL	500	Shift Right Single Logical
SRDL	900	Shift Right Double Logical
SLC	800/1300+ 300•x[2]	Shift Left and Count
AR	500/1000	Add R
ADR	900/1400	Add Double R
ANR	500/1000	Add Negative R
ADNR	900/1400	Add Double Negative R
MR	500/6300	Multiply R
DR	6500/7000	Divide R
REM[6]	500/1000	R Equal
RNEM[6]	500/1000	R Not Equal
RGEM[6]	500/1000	R Greater or Equal
RLSM[6]	500/1000	R Less
DB	15.2/15.7[7]	Decimal to Binary
BD	15.3/15.8[7]	Binary to Decimal
LCR	500/1000	Load Complement R
LNR	500/1000	Load Negative R
LI	500	Load Immediate
AI	500	Add Immediate
ANI	500	Add Negative Immediate
LA	1200/1700	Load A
SA	1200/1700	Store A
MA	*	Multiply A
DA	*	Divide A
FA	*	Floating Add
FAL	*	Floating Add Long
FAN	*	Floating Add Negative
FANL	*	Floating Add Negative Long
FM	*	Floating Multiply
FML	*	Floating Multiply Long
FD	*	Floating Divide
FDL	*	Floating Divide Long
FSC	1600	Force Subsystem Command
SIO	500[8]	Start I/O
TIO	500/1000	Test I/O
HIO	500[9]	Halt I/O
WP	500	Write Pointers
RP	500	Read Pointers
TSS	800/1300	Test Set and Skip
TCS	800/1300	Test Clear and Skip
XQT	700	Execute
STOP	500	Stop
EEI	500	Enable Extended Indexing
DEI	500	Disable Extended Indexing
EI	500	Enable I/O Interrupts
DI	500	Disable I/O Interrupts
ELN	Note 10	Enter Level Number
LCSR	500	Load Channel Select Register
LME	500	Load Manual Entry

NOTES:

1. Where two execution times are given, first represents execution time if skip/jump condition not met; second represents time if skip/jump condition is met.

2. Number of iterations until condition met (x is 1→15).

3. Indirect adds 700 ns to any instruction where indirect is used.

4. Auto Increment or Decrement adds 1200 ns to any instruction where it is used.

5. P relative jump adds 500 ns.

6. Times for unmasked compares (k = 7 mnemonic without M) are identical.

7. Execution times for these instructions in usec.

8. If the I/O paging option is installed, the SIO executed on a non-paged channel requires 1.6 usec and an SIO executed on a page channel requires 2.5 usec.

9. 2.2 usec if the Hard Controlled Word Register option is installed.

10. Execution times shown on Table 5.

* Execution times for these instructions will be furnished at a later date.

WAICOM-16 REAL-TIME SYSTEM SUMMARY

The modular construction of WAICOM-16 hardware and Executive operating system features allow the user to configurate the total system to meet his specific needs. A brief summary of these features and their operation follows:

INTERRUPTS

Interrupts originating in the I/O section are classified in one of three ways: (1) either the interrupt is critical to system operation requiring immediate software attention (hard), (2) the interrupt is of less importance and need not be handled immediately (soft), or (3) the interrupt is the result of a detected error during a critical I/O operation (fault). Hard interrupts allow control to be transferred to the appropriate user task. Soft interrupts are processed by the Executive dispatcher on a deferred basis according to their eligibility and priority.

I/O CONTROL

The Input/Output section of the processor controls transfers of data over I/O channels between memory and peripheral subsystems. I/O transfers in and out of memory share a path to memory with operand loads and stores in the processor. The I/O transfer cycle takes priority over the operand cycle. The I/O cycle may occur simultaneously with an instruction fetch (exclusive of a jumped to instruction fetch which uses the operand path) if the instruction and I/O word are in physically different 8K memory modules. Since there are a minimum of instructions using memory operands, I/O transfers have a minimum effect on program execution.

PRIORITY OPERATION

Any number of I/O channels may have transfers in progress concurrently and the requests from each channel occur asynchronously with respect to each other and to any sequence within the processor. It is therefore, necessary to establish a priority for servicing requests. The following lists the priorities which are established from highest to lowest priority:

Storage Fault
Channel Requests
Soft Interrupt Control Word Expiration
I/O Instructions: Halt I/O, Force Subsystem Command, and Start I/O (if paged channel)
Real Time Clock

MULTI-TASK OPTION

The multi-task option is intended for use when several users share a processor and each user desires complete user integrity.

This feature enables a user to protect his program from other users, and to protect portions of user memory space from user operations.

The multi-task option is implemented by assigning level numbers to each user's task, under software control. The level number assigned to a program defines to some extent the privilegeness of the program. Levels 0 through 3 have the privilege of specifying input-output channel numbers and, executing all instructions, and shifting directly from one level to another.

Level numbers 4 through 7 are of the user class; however input/output instructions may be executed in these levels on input/output channels specified by a level 0 through 3 program.

Level numbers 8 through 31 are for user programs where execution of privileged instructions causes a fault and program control reverts to an executive level.

SUMMARY

The man-machine interface features of the WAICOM-16 provide a Real-Time system encompassing time-sharing and process control requirements, as well as normal data processing needs.

For more information contact:

Weismantel Associates, Inc.
Marketing
Box 1957
St. Paul, Minnesota 55111

WEISMANTEL ASSOCIATES INC., BOX 1957, ST. PAUL, MINNESOTA 55111

LITHO USA 4/70

W1012